

PXI Express

NI PXIe-6674T User Manual

Timing and Synchronization Module for PXI Express

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While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC¹.

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments such as, for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC¹ for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments could void the user's right to operate the hardware under the local regulatory rules.

¹ The Declaration of Conformity (DoC) contains important EMC compliance information and instructions for the user or installer. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

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About This Manual

Thank you for purchasing the National Instruments NI PXIe-6674T Timing and Synchronization Module. The NI PXIe-6674T enables you to pass PXI timing and trigger signals between PXI Express chassis. The NI PXIe-6674T can generate and route clock signals between devices in multiple chassis, providing a method to synchronize multiple devices in a multichassis PXI Express system.

This manual describes the electrical and mechanical aspects of the NI PXIe-6674T and contains information concerning its operation and programming.

National Instruments Documentation

The *NI PXIe-6674T User Manual* is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Refer to the *NI-Sync User Manual*, available at ni.com/manuals.

You can download NI documentation from ni.com/manuals.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0, CompactPCI Core Specification*, available from PICMG at www.picmg.org
- *PXI Specification*, Revision 2.1, available from www.pxisa.org
- *NI-VISA User Manual*, available from ni.com/manuals
- *NI-VISA Help*, included with the NI-VISA software
- *NI-Sync User Manual*, available from ni.com/manuals
- *NI PXIe-6674T Calibration Procedure*, available from ni.com/manuals

Introduction

The NI PXIe-6674T timing and synchronization module enables you to share clock and triggers between modules in a PXI Express chassis and other PXI chassis or non-PXI systems. The NI PXIe-6674T module generates and routes clock signals between devices in multiple chassis, providing a method for synchronizing multiple devices in a PXI Express system. It also features a precision OCXO for improving the stability and accuracy of the PXI Express backplane reference clocks.

What You Need to Get Started

To set up and use the NI PXIe-6674T, you need the following items:

- ☐ NI PXIe-6674T Timing and Synchronization Module
- ☐ [NI PXIe-6674T User Manual](#)
- ☐ *NI-Sync* CD
- ☐ One of the following software packages and documentation:
 - LabVIEW
 - LabWindows™/CVI™
 - Microsoft Visual C++ (MSVC)
- ☐ PXI EMC filler panels, National Instruments part number 778700-01
- ☐ PXI Express chassis
- ☐ PXI Express embedded controller or a desktop computer connected to the PXI Express chassis using MXI-Express hardware

The *NI-Sync User Manual* offers more detailed information on the software used to program the NI PXIe-6674T. You can find this manual on the *NI-Sync* CD or download it from ni.com/manuals.

Unpacking

The NI PXIe-6674T is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage the module.



Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. *Do not* install a damaged module into the computer.

Store the NI PXIe-6674T in the antistatic envelope when not in use.

Software Programming Choices

When programming the NI PXIe-6674T, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do not operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do not substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product *must* be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate the product at or below the measurement category¹ marked on the hardware label. Measurement circuits are subjected to working voltages² and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS³ voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS³). This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 AC voltage

¹ Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

² Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

³ MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.

- Measurement Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Measurement Category IV is for measurements performed at the primary electrical supply installation typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

Installing and Configuring

This chapter describes how to install the NI PXIe-6674T hardware and software and how to configure the device.

Installing the Software

Refer to the `readme.htm` file that accompanies the *NI-Sync* CD for software installation directions.



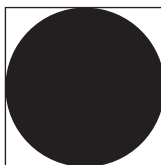
Note Be sure to install the driver software *before* installing the NI PXIe-6674T hardware.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Locate the system timing slot for your PXI Express chassis. It is identified by the glyph shown in Figure 2-1.

Figure 2-1. System Timing Slot Indicator Glyph



3. Remove the filler panel for the system timing slot, if applicable.
4. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the [Unpacking](#) section of Chapter 1, [Introduction](#).
5. Carefully insert the NI PXIe-6674T into the system timing slot making sure to not scrape the module on any adjacent modules. Use the injector/ejector handle to fully insert the module into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the chassis.
7. If adjacent slots are not populated, use EMC filler panels to cover the opening.



Caution To ensure the specified EMC performance, you must install PXI EMC filler panels, National Instruments part number 778700-01, in all open chassis slots.

8. Visually verify the installation. Ensure that the module is fully inserted into the slot.
9. Plug in and power on the chassis.

The NI PXIe-6674T is now installed.

Configuring the Module

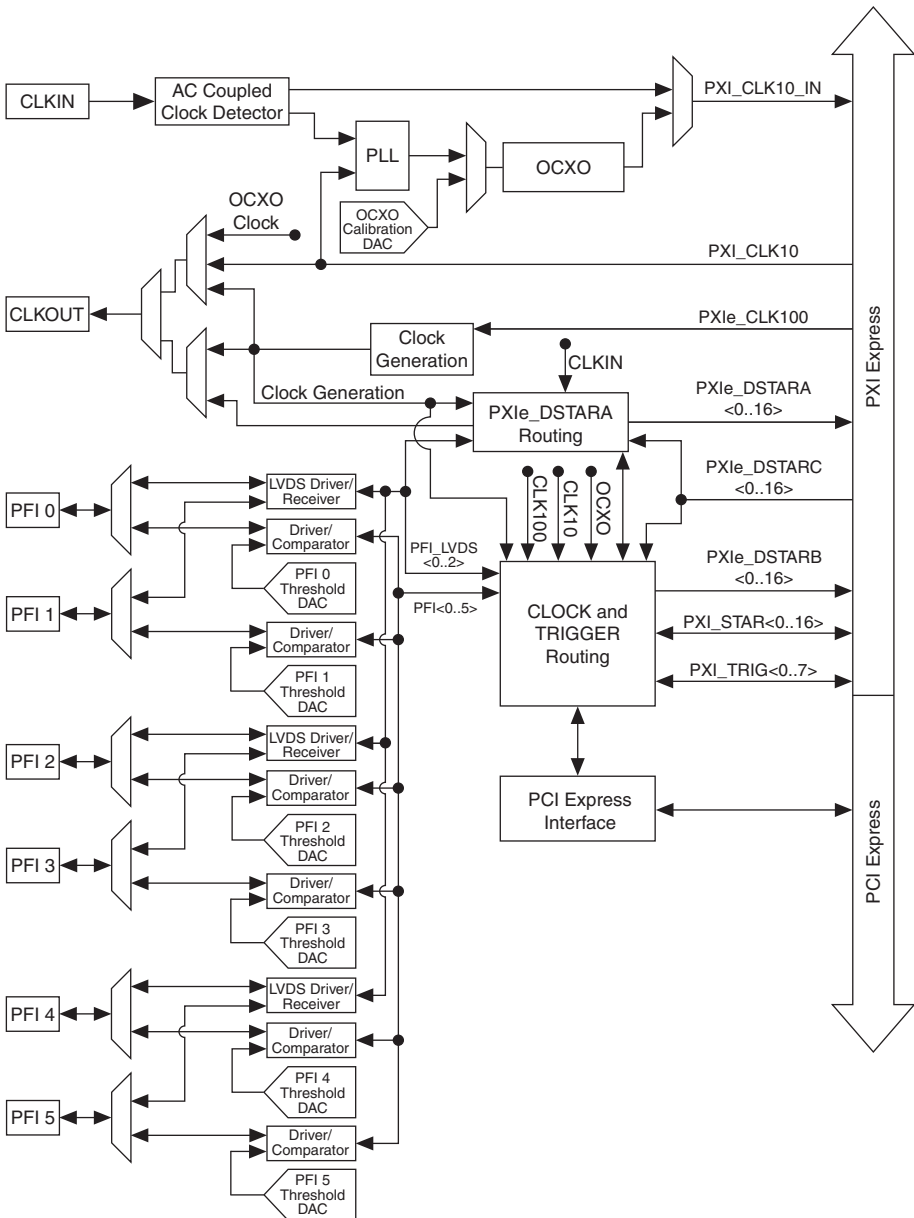
The NI PXIe-6674T is completely software configurable. The system software automatically allocates all module resources.

The two LEDs on the front panel provide information about module status. The front panel description sections of Chapter 3, [Hardware Overview](#), describe the LEDs in greater detail.

Hardware Overview

This chapter presents an overview of the hardware functions of the NI PXIe-6674T. Figure 3-1 provides a functional overview of the NI PXIe-6674T hardware.

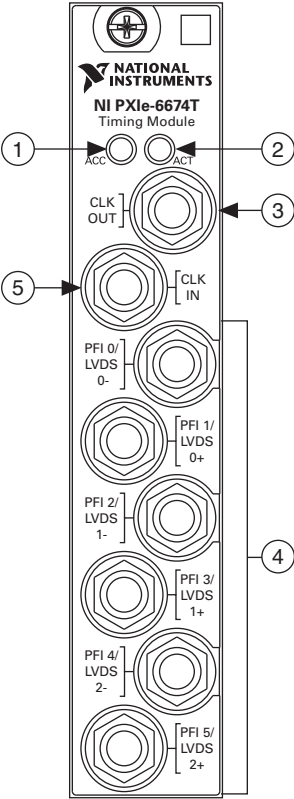
Figure 3-1. Functional Overview of the NI PXIe-6674T



NI PXIe-6674T Front Panel

Figure 3-2 shows the connectors and LEDs on the front panel of the NI PXIe-6674T.

Figure 3-2. NI PXIe-6674T Front Panel



- | | |
|--------------------|------------------------|
| 1 Access LED | 4 PFI<0..5> Connectors |
| 2 Active LED | 5 CLKIN Connector |
| 3 CLKOUT Connector | |

Access LED

The Access LED indicates the communication status of the NI PXIe-6674T. Refer to Figure 3-2 for the location of the Access LED.

Table 3-1 summarizes what the Access LED colors represent.

Table 3-1. Access LED Color Indication

Color	Status
Off	Module is not yet functional.
Green	Driver has initialized the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.
Blinking Red	Module has detected an over-temperature condition.
Solid Red	A hardware error has been detected.



Caution If the Access LED is observed to be blinking red, the module has detected an over-temperature condition. Continued use of the NI PXIe-6674T in this condition is not recommended as product reliability may become comprised. Since several common problems can cause an over-temperature condition, please investigate the following:

- Check that all chassis covers, filler panels, and/or slot blockers are installed.
- Make sure that the chassis fan speed is set to the highest setting.
- If applicable, check that the chassis fan air intake is not blocked and that the fan filters are clean.
- Make sure that the ambient temperature around the chassis isn't above the rated temperature specifications. If so, move the chassis to a cooler ambient temperature location.



Caution If the Access LED is observed to be solid red, a hardware failure has been detected that may impact the performance of the NI PXIe-6674T. Contact National Instruments for support.

Active LED

The Active LED indicates an error or phase-locked loop (PLL) activity. You can change the Active LED to amber, unless an error overrides the selection. Refer to Figure 3-2 for the location of the Active LED.



Tip Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis situation or when you want an indication that your application has reached a predetermined section of the code.

Table 3-2 summarizes what the Active LED colors represent.

Table 3-2. Active LED Color Indication

Active LED Color	Status
Off	The 10 MHz PLL is not in use and no errors are present.
Green	The 10 MHz PLL is active and locked.
Solid Amber	The user can set the Active LED to amber through software.
Solid Red	10 MHz PLL is attempting to lock to the reference supplied on CLKIN.

Connectors

This section describes the connectors on the front panel of the NI PXIe-6674T.

- **CLKIN**—AC coupled, 50 Ω clock input. CLKIN can be routed directly to PXI_CLK10_IN, to the 10 MHz PLL, to PXIe_DSTARA, or to the FPGA for use as a synchronization clock.
- **CLKOUT**—AC coupled clock output. CLKOUT can be sourced from the OCXO, PXI-CLK10, Clock Generation, or from the PXIe_DSTARA network.
- **PFI<0..5>/PFI_LVDS<0..2>**—Programmable Function Interface which can be individually configured for either single ended operation or LVDS operation. In LVDS mode, the connectors are paired and can be programmatically set as either inputs or outputs, but not both simultaneously.

Refer to Figure 3-2 for a diagram showing the locations of these connections on the NI PXIe-6674T front panel.



Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXIe-6674T can damage the module and the computer. NI is *not* liable for any damage resulting from such signal connections.

Hardware Features

The NI PXIe-6674T performs two broad functions:

- Generating clock and trigger signals
- Routing internally or externally generated signals from one location to another

Table 3-3 outlines the function and direction of the signals discussed in detail in the remainder of this chapter.

Table 3-3. Signal Descriptions

Signal Name	Direction	Description
PXI_CLK10_IN	Out (to chassis)	This is a signal that can be used to provide the backplane with a reference 10 MHz signal from the system timing slot. When a 10 MHz signal is connected to PXI_CLK10_IN, the PXI Express chassis is required to derive PXI_CLK10 and PXIe_CLK100 from this reference. Refer to the user manual for your PXI Express chassis for more information on how it uses PXI_CLK10_IN.
PXI_CLK10	In (from chassis)	This signal is the PXI 10 MHz backplane clock. This signal is the output of the native 100 MHz oscillator in the chassis divided by ten.
PXIe_CLK100	In (from chassis)	This signal is the PXI Express 100 MHz backplane clock. PXIe_CLK100 offers tighter slot to slot timing than PXI_CLK10.
OCXO Clock	Out (internal)	This is the output of the 10 MHz OCXO. The OCXO is an extremely stable and accurate frequency source.
CLKIN	In (from front panel)	CLKIN is the signal connected to the SMA input connector of the same name. CLKIN can be routed directly to PXI_CLK10_IN, to the 10 MHz PLL, to PXIe_DSTARA, or to the FPGA.
CLKOUT	Out (to front panel)	CLKOUT is the signal on the SMA output connector of the same name. CLKOUT can be sourced from the OCXO, PXI_CLK10, Clock Generation, or from the PXIe_DSTARA network.

Table 3-3. Signal Descriptions (Continued)

Signal Name	Direction	Description
Clock Generation	Out (internal)	Clock Generation refers to the clock signal coming from the onboard clock generation circuitry of the NI PXIe-6674T. The clock generation circuitry can generate a clock from sub-1 Hz to 1 GHz with fine granularity and is automatically locked in phase to PXIe_CLK100.
PFI<0..5>	In/Out (to/from front panel)	The single ended Programmable Function Interface pins on the NI PXIe-6674T route timing and triggering signals between multiple PXI Express chassis. A wide variety of input and output signals can be routed to or from the PFI lines.
PFI_LVDS<0..2>	In/Out (to/from front panel)	The LVDS Programmable Function Interface can be used to route timing and triggering signals between multiple PXI Express chassis. The use of LVDS logic allows much faster speeds than can be achieved with the single ended PFIs. The LVDS PFIs when used as outputs can be sourced from the PXIe_DSTARA network, the FPGA, or the clock generation circuitry. As inputs the LVDS PFIs can be routed to the PXIe_DSTARA network and to the FPGA.
PXI_TRIG<0..7>	In/Out (to/from chassis)	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI Express chassis. The NI PXIe-6674T can route a wide variety of signals to and from these lines. Note: PXI_TRIG<0..5> are also known as RTSI<0..5> in some hardware devices and APIs. However, PXI_TRIG<6..7> are <i>not</i> identical to RTSI<6..7>.
PXI_STAR<0..16>	In/Out (to/from chassis)	The PXI star trigger bus connects the system timing slot to other peripheral slots in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. An NI PXIe-6674T in the system timing slot can route signals to all available PXI_STARS in the PXI Express chassis.

Table 3-3. Signal Descriptions (Continued)

Signal Name	Direction	Description
PXIE_DSTARA	Out (to chassis)	The PXIE_DSTARA lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to distribute a clock signal to every slot. PXIE_DSTARA uses differential LVPECL signaling and is capable of high speed clock distribution. Refer to the PXIE_DSTARA Network section for more information.
PXIE_DSTARB	Out (to chassis)	The PXIE_DSTARB lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to send out high speed triggers to every slot. PXIE_DSTARB uses differential LVDS signaling and is capable of sending out higher speed trigger signals.
PXIE_DSTARC	In (from chassis)	The PXIE_DSTARC lines connect each peripheral slot in a PXI Express chassis to the system timing module, allowing the system timing module to receive high speed clock and trigger signals from every slot. PXIE_DSTARC uses differential LVDS signaling.

The remainder of this chapter describes how these signals are used, acquired, and generated by the NI PXIE-6674T hardware, and explains how you can route the signals between various locations to synchronize multiple measurement devices and PXI chassis.

Generating and Routing Clocks

The NI PXIE-6674T can generate two types of clock signals. The first clock is generated using the onboard clock generation circuitry, and the second is generated with a precise 10 MHz oscillator. The following sections describe the two types of clock generation and explain the considerations for choosing either type.

Clock Generation

The NI PXIE-6674T includes built-in advanced clock generation circuitry for generating clock signals from below 1 Hz to 1 GHz with very fine frequency resolution. The clock generation circuitry is based on a direct digital synthesis (DDS) with an 800 MHz reference phase locked to PXIE_CLK100. This allows the DDS to generate a 150 MHz-300 MHz signal with microhertz resolution. The output from the DDS can then be divided down to lower frequencies, used directly, or multiplied up using a phase locked voltage controlled oscillator.

The individual components which make up the clock generation circuitry are controlled by NI-Sync software, which allows the user to simply specify the frequency they wish the clock generation circuitry to produce. NI-Sync will then configure the clock generation circuitry to give the closest possible frequency match to the requested frequency and do so with the configuration that gives the lowest possible phase noise. The user may request a clock frequency up to 1 GHz (frequencies beyond 1 GHz are possible but performance is not specified). The precision of the frequency generated is that of the DDS scaled up or down for any division or multiplication done to generate the requested frequency, as shown in Table 3-4.

Table 3-4. Resolution by Frequency Range

Clock Generation Frequency	Resolution
18.75 MHz to 37.5 MHz	0.355 μ Hz
37.5 MHz to 75 MHz	0.711 μ Hz
75 MHz to 150 MHz	1.42 μ Hz
150 MHz to 300 MHz	2.84 μ Hz
300 MHz to 600 MHz	5.68 μ Hz
600 MHz to 1 GHz	11.4 μ Hz

Because the 800 MHz reference of the clock generation circuitry is phase locked to PXIe_CLK100, its frequency accuracy is inherited from PXIe_CLK100. To give the best frequency accuracy, the OCXO of the NI PXIe-6674T can be routed to PXI_CLK10_IN which the chassis can then use to lock PXIe_CLK100 and PXI_CLK10. In addition, using the OCXO will also lower the phase noise of the generated clock frequency.

PXI_CLK10 and PXIe_CLK100

The PXI Express architecture allows a module in the system timing slot to provide a 10 MHz reference clock to the backplane for use in creating PXI_CLK10 and PXIe_CLK100. This is done by using the PXI_CLK10_IN pin on the backplane connector.

Most PXI Express backplane architectures employ a PLL to lock a 100 MHz reference oscillator to the signal coming from PXI_CLK10_IN pin. This 100 MHz reference is then used to directly create PXIe_CLK100 and is divided down by ten to create PXI_CLK10. This architecture has the advantage that PXI_CLK10 and PXIe_CLK100 are always sourced from the same reference oscillator, and therefore it is impossible to lose PXI_CLK10 or PXIe_CLK100 by disconnecting the reference provided on PXI_CLK10_IN. For the same reason, it is also impossible for a runt pulse or glitch to occur on these lines as references are switched in and out, protecting the integrity of digital circuitry operating on these clocks. Another feature of this architecture is that the phase noise performance of PXI_CLK10 and PXIe_CLK100 is fixed beyond the bandwidth of the PLL loop of the backplane, regardless of the quality of the reference used. This is

advantageous if a reference with poor phase noise performance is used, but it also means that supplying a high end low phase noise reference will not greatly improve PXI_CLK10 or PXIe_CLK100.

Using PXI_CLK10_IN

The NI PXIe-6674T provides three options for driving a clock to the backplane using PXI_CLK10_IN: OCXO, CLKIN, and 10 MHz PLL.

OCXO

The NI PXIe-6674T features a precision 10 MHz Oven Controlled Crystal Oscillator (OCXO). The main source of frequency error in reference oscillators is temperature variation. An OCXO minimizes this error by housing the crystal oscillator circuit inside a sealed oven, which is maintained at a constant temperature higher than the ambient temperature external to the OCXO. This results in a reference oscillator that is several orders of magnitude more stable and accurate than regular crystal oscillators.

Because the OCXO must warm up to a higher temperature than the ambient temperature around it, there is a warm up time required to achieve the specified frequency accuracy. For this reason, to achieve the most stable operation of the OCXO it is desirable to avoid powering off the OCXO.

The OCXO used by the NI PXIe-6674T features electronic frequency control. This allows the OCXO to be fine-tuned by varying the control voltage to the OCXO. The NI PXIe-6674T uses a 16-bit digital analog converter to give precise control of the tuning voltage. While the tuning voltage can be varied by the user, it is normally controlled automatically by software which sets it to the calibration tuning voltage. The NI PXIe-6674T is calibrated during the manufacturing process and should be recalibrated annually to remove frequency error that accumulates over time (such as crystal aging). Refer to the *NI PXIe-6674T Calibration Procedure* at ni.com/calibration for more details.

The OCXO can also be routed to the CLKOUT SMA and be used as a trigger synchronization clock inside the FPGA.

CLKIN

The NI PXIe-6674T allows the user to connect their own 10 MHz reference directly to PXI_CLK10_IN by using the CLKIN SMA on the front panel. CLKIN is an AC coupled, 50 Ω terminated input to the NI PXIe-6674T. In order to increase the amplitude of signals the CLKIN receiver can use, the CLKIN circuitry features software enabled attenuation, which when enabled will attenuate the input signal by a factor of five. NI-Sync software will by default configure the attenuation to be enabled. If the input signal supplied to CLKIN is less than 1.2 V_{pp}, the attenuation should be turned off in order to extend down the range of amplitudes CLKIN can receive.

When using CLKIN for driving PXI_CLK10_IN, please refer to the user manual for your PXI Express chassis for information on the frequency range your chassis is capable of receiving on PXI_CLK10_IN.

CLKIN can also be routed to the DSTARA network and be used as a trigger synchronization clock inside the FPGA.

10 MHz PLL

The NI PXIe-6674T features a phase locked loop (PLL) circuit for aligning the frequency of the OCXO with a reference clock supplied by the user from CLKIN. In this configuration, the OCXO is routed to the backplane on PXI_CLK10_IN. The PXI Express backplane will in turn phase lock the PXI_CLK10 and PXIe_CLK100 signal to the PXI_CLK10_IN signal. The NI PXIe-6674T uses the PXI_CLK10 signal it receives from the backplane as the feedback to the 10 MHz PLL circuitry. The PLL circuitry controls the frequency of the OCXO by varying the tuning voltage used for the electronic frequency control. By increasing or decreasing the frequency of the OCXO as needed, the 10 MHz PLL of the NI PXIe-6674T is able to match the OCXO frequency to the reference clock supplied by the user from CLKIN.

Use of the 10 MHz PLL of the NI PXIe-6674T has advantages over using just CLKIN to drive PXI_CLK10_IN:

- Reference frequencies other than 10 MHz can be used. The 10 MHz PLL includes internal dividers to divide both the reference from CLKIN and PXI_CLK10 down as needed in order to make both a common frequency. This frequency is called the phase detector frequency, as it is the frequency at which the PLL compares edge alignment to determine if it should speed up or slow down the OCXO. NI-Sync allows any reference frequency that is an integer multiple of 1 MHz to be used.
- The 10 MHz PLL acts as a zero-delay buffer between the CLKIN SMA and PXI_CLK10/PXIe_CLK100 at the backplane connector. Because the 10 MHz PLL uses PXI_CLK10 for feedback, it is able to create a known fixed phase relation between PXI_CLK10 and the reference supplied on CLKIN. During manufacturing, the phase relation the 10 MHz PLL maintains is adjusted so that a rising edge at the CLKIN SMA will align in time with a rising edge of PXI_CLK10 at the peripheral slot connector of the backplane. This phase relation will remain in place regardless of the PXI Express chassis used, allowing for simpler multi-chassis system synchronization.

PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC

The PXI Express architecture includes a set of three high speed differential signal paths to connect the system timing slot to each PXI Express peripheral slot (up to 17 peripheral slots). These signals are PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC.

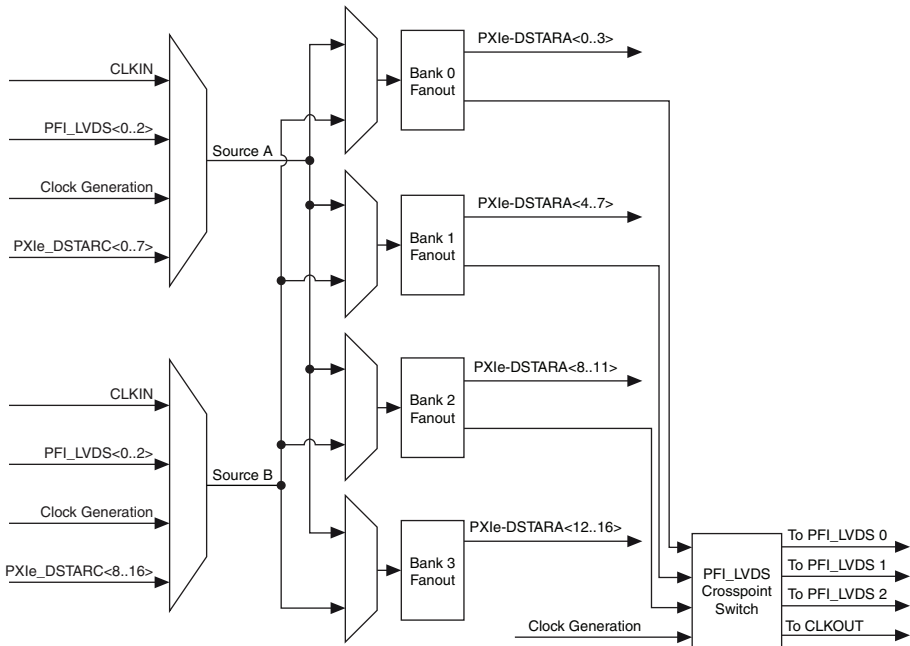
- **PXIe_DSTARA**—PXIe_DSTARA is used to send clock signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARA uses LVPECL signaling and closely matched trace lengths to achieve low skew, high speed clock routing capabilities. Refer to the [PXIe_DSTARA Network](#) section for details on how the NI PXIe-6674T implements PXIe_DSTARA.

- PXle_DSTARB**—PXle_DSTARB is used to send trigger signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXle_DSTARB uses LVDS signaling and closely matched trace lengths to achieve faster, more precise triggering than is achievable with PXI_STAR or PXI_TRIG.
- PXle_DSTARC**—PXle_DSTARC is used to send trigger signals from each PXI Express peripheral slot to the system timing slot in a star configuration. PXle_DSTARC uses LVDS signaling and closely matched trace lengths and can be used to send a trigger signal or clock signal to the system timing slot module. The NI PXIe-6674T receives each PXle_DSTARC signal and sends a copy to the PXle_DSTARA network for clock sharing and to the FPGA for trigger routing.

PXle_DSTARA Network

To achieve the high speed, low skew routing performance required for PXle_DSTARA, the NI PXIe-6674T uses circuitry specifically designed for routing clock signals to PXle_DSTARA<0..16>. NI-Sync software automatically handles the routing through the PXle_DSTARA network. However, because the PXle_DSTARA Network limits the number of connections that can be made, it is important to understand the underlying hardware architecture. Figure 3-3 provides an overview of the PXle_DSTARA network.

Figure 3-3. PXle_DSTARA Network



The PXIe_DSTARA network allows the user to select which source to route to the PXIe_DSTARA lines. It does this by creating two intermediate sources, Source A and Source B. Source A and Source B are created by multiplexers with the source options shown in Table 3-5.

Table 3-5. Sources for Source A and Source B

Inputs to Source A	Inputs to Source B
CLKIN	CLKIN
PFI_LVDS<0..2>	PFI_LVDS<0..2>
Clock Generation	Clock Generation
PXIe_DSTARC<0..7>	PXIe_DSTARC<8..16>

To drive signals out on the PXIe_DSTARA lines, the PXIe_DSTARA network divides the 17 PXIe_DSTARA lines into four banks, as shown in Table 3-6.

Table 3-6. PXIe_DSTARA Divisions

Bank 0	Bank 1	Bank 2	Bank 3
PXIe_DSTARA <0..3>	PXIe_DSTARA <4..7>	PXIe_DSTARA <8..11>	PXIe_DSTARA <12..16>
PFI_LVDS cross point	PFI_LVDS cross point	PFI_LVDS cross point	—

Each one of the Banks can select from either Source A or Source B and all the PXIe_DSTARA lines that a Bank drives out must share the same source. Banks 0, 1, and 2 send a copy of their output to the PFI_LVDS cross point switch for routing out the front panel using the PFI lines in LVDS mode. Refer to the [PFI_LVDS<0..2>](#) section for more information.



Note Because a single integrated circuit is used to make the five outputs in each bank, tighter skew is achieved within a single Bank than from Bank to Bank.

PFI_LVDS<0..2>

To allow for sending and receiving signals between system timing modules that are too fast for single ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. Table 3-7 shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

Table 3-7. Combinations of PFI Lines for PFI_LVDS

PFI Line	PFI_LVDS Line
PFI 0	PFI_LVDS 0 Negative
PFI 1	PFI_LVDS 0 Positive
PFI 2	PFI_LVDS 1 Negative
PFI 3	PFI_LVDS 1 Positive
PFI 4	PFI_LVDS 2 Negative
PFI 5	PFI_LVDS 2 Positive

Each of the three PFI_LVDS can be enabled for LVDS operation or used for two single ended PFIs. When enabled for LVDS operation, the PFI_LVDS pair can be configured as either an input or an output. PFI_LVDS lines can not be used as an input and output at the same time.

Because of the increased speed capabilities, the PFI_LVDS include additional routing capabilities not offered with the single ended PFI. When used as in an input, the PFI_LVDS signal goes to both the FPGA for trigger routing and to the PXIe_DSTARA Network for use in routing high speed clocks. When used as an output, the PFI_LVDS can be sourced from the FPGA for trigger usage, or from a 4x4 cross point switch which allows for any of the four inputs to be connected to any of the four outputs. Table 3-8 shows the inputs and outputs of the cross point switch.

Table 3-8. Inputs and Outputs of the Cross Point Switch

Inputs	Outputs
PXIe_DSTARA Network Bank 0	PFI_LVDS 0
PXIe_DSTARA Network Bank 1	PFI_LVDS 1
PXIe_DSTARA Network Bank 2	PFI_LVDS 2
Clock Generation	High Speed CLKOUT

If the PFI_LVDS output is used for trigger routing, it is sourced from the FPGA and has all the same trigger routing characteristics as other trigger destinations. Refer to the [Using Front Panel PFIs for LVDS Triggers](#) section for details on using PFI_LVDS for sending and receiving trigger signals.

CLKOUT

The CLKOUT SMA connector on the front panel provides a means to export a clock signal from the NI PXIe-6674T to an external device or another system timing module. The CLKOUT driver uses two separate circuits for driving CLKOUT, one for low speed frequencies (50 MHz and below) and one for high speed (above 50 MHz). The low speed driver uses 5 V CMOS logic with source impedance of 50 Ω and is AC coupled. The high speed driver produces an 800 mV_{pp} swing into a 50 Ω load and is also AC coupled.

The sources available to be routed to CLKOUT differ depending on whether the low speed or high speed driver is used. The sources available to the low speed driver are PXI_CLK10, OCXO, and Clock Generation for generated frequencies 100 MHz and below. Sources available to the high speed CLKOUT are Clock Generation and outputs from the PXIe_DSTARA network through the PFI_LVDS cross point switch.

NI-Sync software will select the low speed or high speed driver automatically based on the source connected to CLKOUT.

Routing Signals

The NI PXIe-6674T has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI star triggers, the PXI triggers, and PXIe_DSTARB/PXIe_DSTARC.

Figures 3-4 and 3-5 summarize the routing features of the NI PXIe-6674T. The remainder of this chapter details the capabilities and constraints of the routing architecture.

Figure 3-4. High-Level Schematic of NI PXIe-6674T Signal Routing Architecture

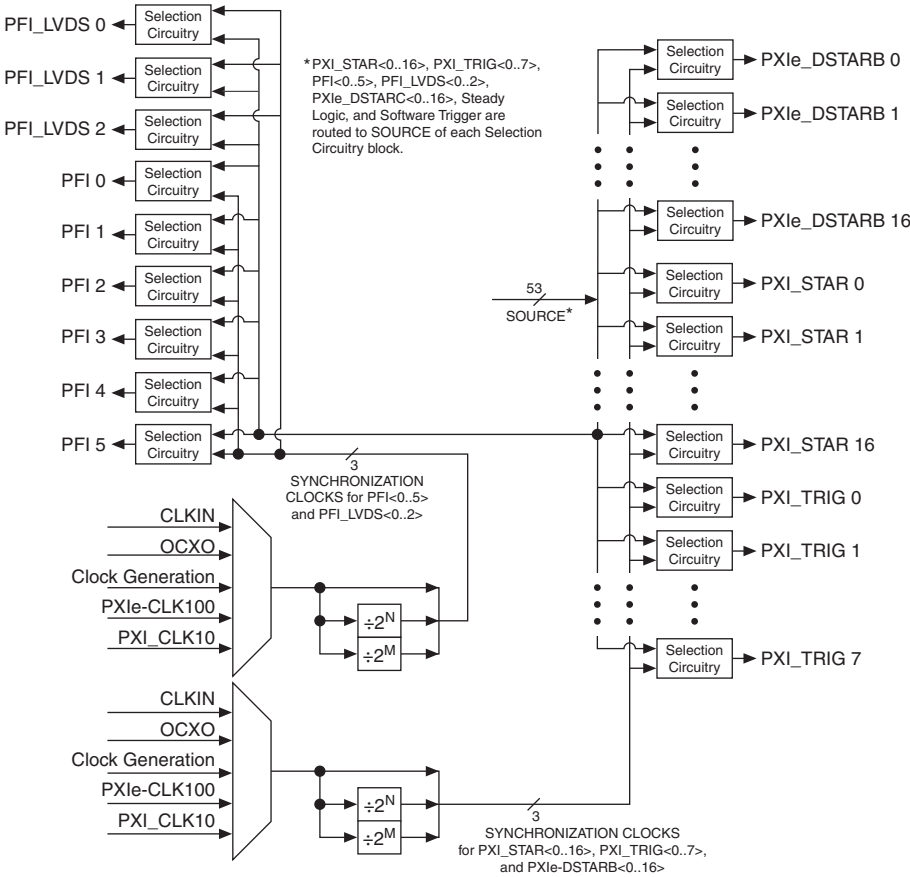
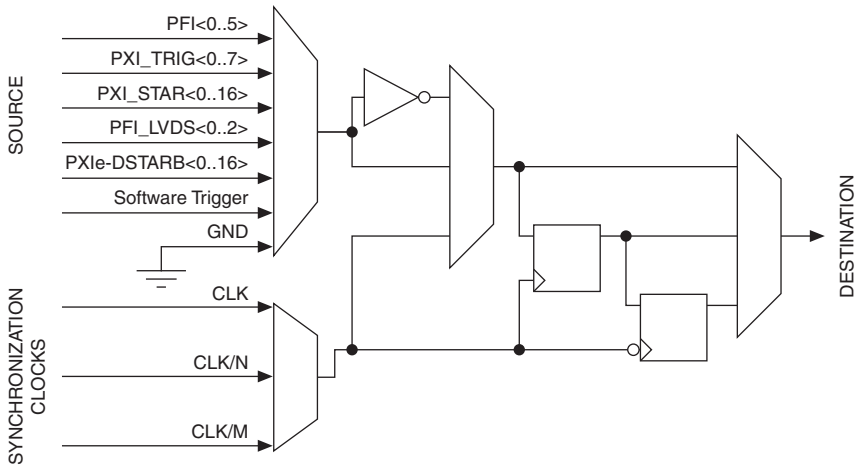


Figure 3-5 provides a more detailed view of the *Selection Circuitry* referenced in Figure 3-4.

Figure 3-5. Signal Selection Circuitry Diagram



Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the [Choosing the Type of Routing](#) section for more information on synchronous versus asynchronous routing.

Table 3-9 summarizes the sources and destinations of the NI PXIe-6674T. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A ✓ in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

Table 3-9. Sources and Destinations for NI PXIe-6674T Signal Routing Operations

Sources	Destinations											
			Front Panel			Backplane						On board
	Front Panel		CLK OUT	PFI <0..5>	PFI LVDS <0..2>	PXI CLK 10 IN	PXI Star Trigger <0..16>	PXI TRIG <0..7>	PXIe SYNC CTRL	D STARA <0..16>	D STARB <0..16>	OCXO Ref PLL
		CLK IN	✓	✓†	✓†	✓	✓†	✓†		✓	✓†	✓
		PFI<0..5>		✓	✓		✓	✓	✓		✓	
PFI LVDS <0..2>			✓	✓		✓	✓	✓	✓	✓		

Table 3-9. Sources and Destinations for NI PXIe-6674T Signal Routing Operations (Continued)

Sources	Destinations											
	Backplane	PXI CLK 10	✓	✓†	✓†		✓†	✓†			✓†	
		PXI CLK 100	✓	✓†	✓†		✓†	✓†			✓†	
		PXI STAR <0..16>		✓	✓		✓	✓	✓		✓	
		PXI TRIG <0..7>		✓	✓		✓	✓	✓		✓	
		DSTARC <0..16>		✓	✓		✓	✓	✓	✓	✓	
	Onboard	OCXO	✓	✓†	✓†	✓	✓†	✓†			✓†	
		Clock Gen	✓	✓†	✓		✓†	✓†		✓	✓†	
		Global Software Trigger		✓	✓		✓	✓	✓		✓	
† Routing PXI_CLK10, PXIe_CLK100, OCXO or ClkGen is accomplished by setting the synchronization clock (NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.												
Route through the FPGA.												
Route to PFI LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DTARA network when used as a clock.												

Using Front Panel PFIs as Single Ended Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. They can be terminated programmatically with 50 Ω resistances to match the cable impedance and minimize reflections.



Note Terminating the signals with a 50 Ω resistance is recommended when the source is another NI PXIe-6674T or any other source with a 50 Ω output.

The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually programmable, which is useful if you are importing signals from multiple sources with different voltage swings.

Using Front Panel PFIs as Single Ended Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. This cable configuration is the recommended setup to minimize reflections. With this configuration, the receiver sees a single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination.

You also can drive a 50 Ω cable with a high-impedance load. The destination sees a single step to +3.3 V, but the source sees a reflection. This cable configuration is acceptable for low-frequency signals or short cables.

You can independently select the output signal source for each PFI line from one of the following sources:

- Another PFI<0..5>
- Another PFI pair in LVDS mode
- PXI triggers <0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARC
- Steady logic high or low

The PFI synchronization clock may be any of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN

- Any of the previously listed signals divided by the first frequency divider (2^n , up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m , up to 512)

Refer to the [Choosing the Type of Routing](#) section for more information on the synchronization clock.



Note The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using Front Panel PFIs for LVDS Triggers

To allow for sending and receiving signals between system timing modules that are too fast for single ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. Table 3-7 shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

When used for trigger routing, the PFI_LVDS signals are routed to and from the FPGA. You can independently select the output signal source for each PFI_LVDS line from one of the following sources:

- Another PFI<0..5>
- Another PFI pair in LVDS mode
- PXI triggers <0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARC
- Steady logic high or low

The PFI synchronization clock is also used for the PFI_LVDS and as such may be one of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n , up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m , up to 512)

Refer to the [Choosing the Type of Routing](#) section for more information on the synchronization clock.



Note The PFI synchronization clock is the same for all routing operations in which `PFI<0..5>` or `PFI_LVDS<0..2>` is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Triggers

The PXI triggers go to all the slots in the chassis. All modules receive the same PXI triggers, so PXI trigger 0 is the same for the system timing slot as it is for Slot 3, and so on. This feature makes the PXI triggers convenient in situations where you want, for instance, to start an acquisition on several devices at the same time because all modules will receive the same trigger.

The frequency on the PXI triggers should not exceed 5 MHz to preserve signal integrity. The signals do not reach each slot at precisely the same time. A difference of several nanoseconds between slots can occur in an eight-slot chassis. However, this delay is not a problem for many applications

You can independently select the output signal source for each PXI trigger line from one of the following sources:

- `PFI<0..5>`
- `PFI_LVDS<0..2>`
- Another PXI trigger `<0..7>` (`PXI_TRIG<0..7>`)
- `PXI_STAR<0..16>`
- Global software trigger
- Backplane synchronization clock
- `PXIe_DSTARC`
- Steady logic high or low

The backplane synchronization clock may be any of the following signals:

- Clock Generation
- `PXI_CLK10`
- `PXIe_CLK100`
- `OCXO`
- `CLKIN`
- Any of the previously listed signals divided by the first frequency divider (2^n , up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m , up to 512)

Refer to the [Choosing the Type of Routing](#) section for more information about the synchronization clock.



Note The backplane synchronization clock is the same for all routing operations in which PXI_TRIG<0..7>, PXIe_DSTARB<0..16>, or PXI_STAR<0..16> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Star Triggers

There are up to 17 PXI star triggers per chassis. Each trigger line is a dedicated connection between the system timing slot and one other slot. The *PXI Specification*, Revision 2.1, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI Express chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to the system timing slot from a module in another slot or from the system timing slot to the other module.

You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI triggers <0..7> (PXI_TRIG<0..7>)
- Another PXI star trigger line (PXI_STAR<0..16>)
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARC
- Steady logic high or low

Refer to the [Using the PXI Triggers](#) section for more information on the backplane synchronization clock.

Using the PXIe_DSTARB and PXIe_DSTARC Triggers

To improve beyond the performance the PXI Star triggers offer in low skew trigger routing, PXI Express implements PXIe_DSTARB and PXIe_DSTARC triggers. Each PXI Express peripheral slot in a PXI Express chassis has independent PXIe_DSTARB and PXIe_DSTARC connections with the system timing slot module. This allows peripheral modules to send triggers to the system timing module using PXIe_DSTARC and for the system timing module to send triggers to peripheral modules using PXIe_DSTARB. Both PXIe_DSTARB and PXIe_DSTARC are one directional. The *PXI Express Specification* requires PXI Express chassis to limit the skew between any two PXIe_DSTARC routes to 150 ps.

The NI PXIe-6674T receives PXIe_DSTARC and can route it to both the PXIe_DSTARA network for use as a clock source and to the FPGA for use as a trigger source. The NI PXIe-6674T can independently select from the following sources to be routed to PXIe_DSTARB:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI Triggers<0..7> (PXI_TRIG<0..7>)
- PXI Star Triggers (PXI_STAR<0..16>)
- PXIe_DSTARC<0..16>
- Global Software Trigger
- Steady logic high or low
- Backplane synchronization clock

Refer to the [Using the PXI Triggers](#) section for more information on the backplane synchronization clock.

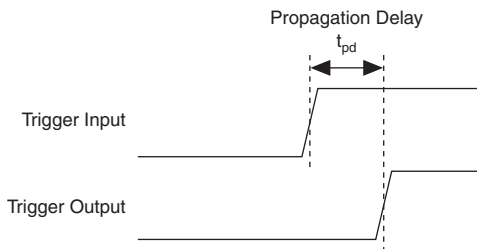
Choosing the Type of Routing

The NI PXIe-6674T routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signal locations: a source and a destination. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. Figure 3-6 illustrates an asynchronous routing operation.

Figure 3-6. Asynchronous Routing Operation



Some delay is always associated with an asynchronous route, and this delay varies among NI PXIe-6674T modules, depending on variations in temperature and chassis voltage. Typical delay times in the NI PXIe-6674T for asynchronous routes between various sources and destinations are given in Appendix A, [Specifications](#).

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source
- Propagation delay of the signal across the backplane(s) and cable(s)
- Propagation delay of the signal through the NI PXIe-6674T
- Time for the receiver to recognize the signal

Both the source and the destination of an asynchronous routing operation on the NI PXIe-6674T can be any of the following lines:

- Any front panel PFI pin (PFI<0..5>) as single ended
- Any front panel PFI pin as LVDS (PFI_LVDS<0..2>)
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARB<0..16>

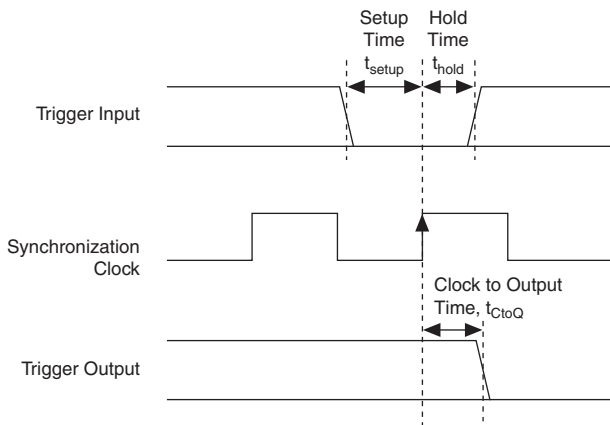
Synchronous Routing

A synchronous routing operation is defined in terms of three signal locations: a source, a destination, and a *synchronization clock*. A digital signal comes in on the source and is propagated to the destination after the edge has been realigned with the synchronization clock.

Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the output waits for the next rising edge of the clock before it follows the input. Thus, the output is said to be “synchronous” with this clock.

Figure 3-7 shows a timing diagram that illustrates synchronous routing.

Figure 3-7. Synchronous Routing Operation



Synchronous routing can send triggers to several places in the same clock cycle. If a signal arrives at two chassis within the same clock cycle, each NI PXIe-6674T realigns the signal with the synchronization clock and distributes it to the modules in each chassis at the same time. Synchronous routing can thus remove uncertainty about when triggers are received. If the delays through the system are such that an asynchronous trigger might arrive near the edge of the receiver clock, the receiver might see the signal in the first clock cycle, or it might see it in the second clock cycle. However, by synchronizing the signal, you can eliminate the ambiguity, and the signal will always be seen in the second clock cycle.

One useful feature of synchronous routing is that the signal can be propagated on either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals.

Possible sources for synchronous routing include the following sources:

- Any front panel PFI pin as single ended
- Any front panel PFI pin as LVDS
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARB<0..16>
- Global software trigger
- The synchronization clock itself

The synchronization clock for a synchronous route can be any of the following signals:

- 10 MHz PXI_CLK10
- 100 MHz PXIe_CLK100
- Clock Generation
- OCXO
- CLKIN
- One of two “divided copies” of any of the previously listed five signals. The NI PXIe-6674T includes two clock-divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

Refer to Figures 3-4 and 3-5 for an illustration of how the NI PXIe-6674T performs synchronous routing operations.

Calibration

This chapter discusses the calibration of the NI PXIe-6674T.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The NI PXIe-6674T is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, [Specifications](#). The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the NI PXIe-6674T involves calculating and storing four calibration constants. These values control the accuracy of two features of the device, which are discussed in the following sections.

OCXO Frequency

The OCXO frequency can be varied over a small range. The output frequency of the OCXO is adjusted using this constant to meet the specification listed in Appendix A, [Specifications](#).

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.



Note The PXI_CLK10 phase is set during manufacturing and does not need to be recalibrated.

Additional Information

Refer to ni.com/calibration for additional information on NI calibration services.

Specifications

This appendix lists the system specifications for NI PXIe-6674T modules. These specifications are typical at 25 °C, unless otherwise stated.



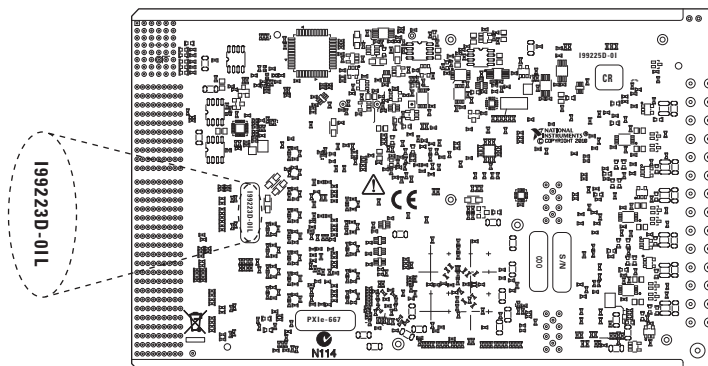
Note Specifications are subject to change without notice.



Note Some specifications are specific to earlier revisions of the NI PXIe-6674T module. A label with revision information can be found on the module board as shown in Figure A-1.

x denotes all letter revisions of the assembly. Ensure the specifications of interest match the revision that is printed on the label.

Figure A-1. NI PXIe-6674T Revision Label



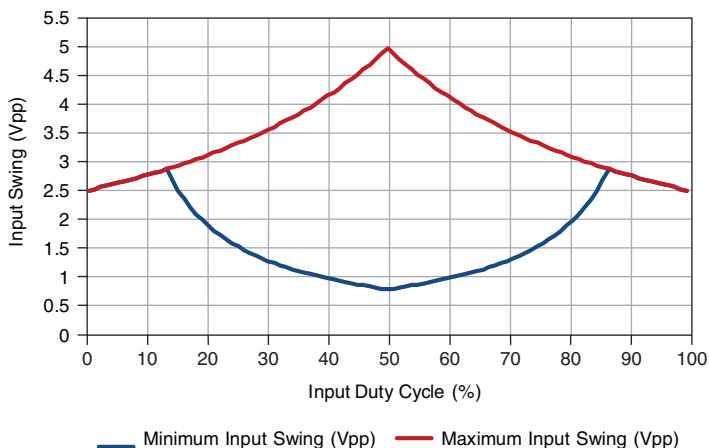
CLKIN Characteristics

Input coupling AC
Input impedance 50 Ω, nominal
Minimum and Maximum Input Levels

Setting	Attenuation Setting On	Attenuation Setting Off
Attenuation Setting	On (default)	Off
Attenuation Behavior	5:1	1:1
Minimum Input Swing with 50% Duty Cycle*	750 mV _{pp}	150 mV _{pp}
Maximum Input Swing with 50% Duty Cycle†	5.0 V _{pp}	1.2 V _{pp}
Absolute Maximum Input Powered On‡	5.6 V _{pp}	2.8 V _{pp}
Absolute Maximum Input Powered Off**	1.5 V _{pp}	
* A duty cycle other than 50% will increase the minimum input swing. Refer to Figure A-2 for more information. † A duty cycle other than 50% will increase the minimum input swing. Refer to Figure A-3 for more information. ‡ Operation above the Absolute Maximum Input Powered On may cause damage to the device. ** Absolute Maximum Input Powered Off is the maximum input signal amplitude that the device can tolerate before damage might occur while in an unpowered state.		



Note Input can be either square wave or sinusoidal.

Figure A-2. Maximum and Minimum Input Swing with Attenuation On**Figure A-3. Maximum and Minimum Input Swing with Attenuation Off**

Minimum frequency 1 MHz¹

Maximum frequency

To Clk10PLL 100 MHz

To FPGA 200 MHz

To PXIe-DStarA 1 GHz

ClkIn to PXI_Clk10_In Delay (PLL not used)

Typical at 25 °C 6.75 ns

Maximum over temperature 14.8 ns

¹ The minimum frequency is limited by AC coupling.

OCXO

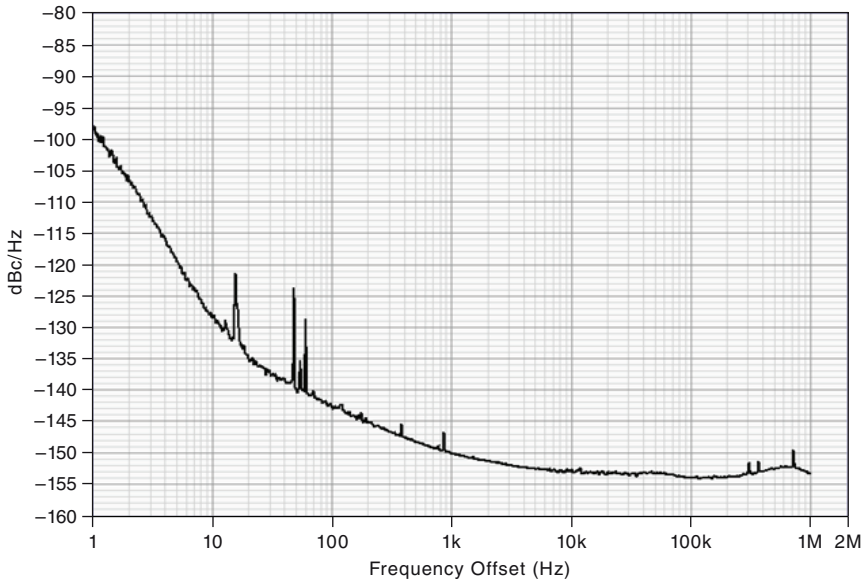
Nominal frequency	10 MHz
Accuracy within 1 year of calibration adjustment within 0 °C to 55 °C	
operating temperature range ¹	±80 ppb
Long-term stability	±50 ppb/year
Stability vs temperature	<10 ppb peak-to-peak within 0 °C to 55 °C operating temperature range
Tuning range	±1.5 ppm minimum, ± 2 ppm typical, ± 4 ppm max
Tuning DAC resolution.....	16 bits, 0.0625 ppb per step typical
Recommended calibration interval	1 year
Maximum Phase Noise of the OCXO	

Offset	Phase Noise
1 Hz	-80 dBc/Hz
10 Hz	-120 dBc/Hz
100 Hz	-140 dBc/Hz
1 kHz	-145 dBc/Hz
10 kHz	-150 dBc/Hz

¹ After 72 hours of continuous operation.

Figure A-4 shows the phase noise on a representative module. OCXO is routed to the ClkOut SMA, measured in a NI PXIe-1082 chassis with low fan speed¹. The integrated jitter from 10 Hz to 1 MHz is 507 fs rms.

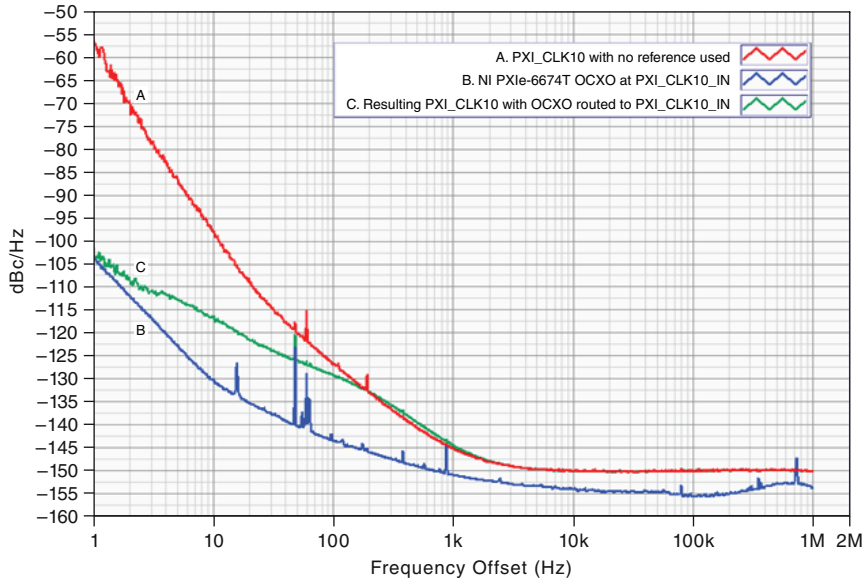
Figure A-4. Phase Noise on a Representative Module with OCXO Routed to ClkOut SMA



¹ OCXO also driven to PXI_CLK10_IN.

Figure A-5 shows the phase noise on a representative module of PXI_CLK10 when OCXO is routed to PXI_CLK10_IN¹, measured in a NI PXIe-1082 chassis with low fan speed:

Figure A-5. Phase Noise on a Representative Module of PXI_CLK10 when OCXO is routed to PXI_CLK10_IN



10 MHz PLL

Reference frequency range

(from ClkIn)..... 1 MHz to 100 MHz, in increments of 1 MHz

Recommended ClkIn frequency² 10 MHz

Reference frequency required accuracy..... ± 1.5 ppm

Reference Frequency Duty Cycle 40% to 60%

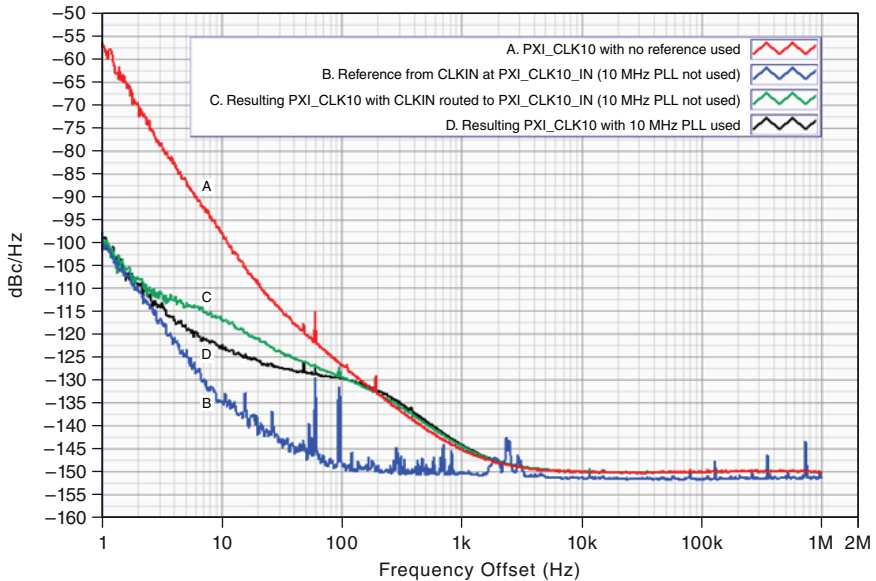
PLL Loop bandwidth 100 Hz

¹ The PXIe backplane employs a PLL to phase lock PXI_CLK10 to the signal on PXI_CLK10_IN. As a result, the phase noise of PXI_CLK10 above about 1 kHz offset is unchanged, regardless of reference used.

² 10 MHz PLL filter is designed for a 10 MHz phase detector frequency. Any other reference frequency will default to a phase detector frequency of 1 MHz resulting in a slight degradation of PLL performance.

Figure A-6 shows the phase noise on a representative module of PXI_CLK10 when CLKIN is routed to PXI_CLK10_IN with and without the 10 MHz PLL, measured in a NI PXIe-1082 chassis with low fan speed¹.

Figure A-6. Phase Noise on a Representative Module of PXI_CLK10 with CLKIN Routing to PXI_CLK10_IN



¹ The PXIe backplane employs a PLL to phase lock PXI_CLK10 to the signal on PXI_CLK10_IN. As a result, the phase noise of PXI_CLK10 above about 1 kHz offset is unchanged, regardless of reference used.

ClkOut

	Low Speed ClkOut	High Speed ClkOut
Coupling	AC Coupled	AC Coupled
Expected Termination	50 Ω or high impedance	50 Ω
Frequency Range	1 MHz to 50 MHz*	1 MHz to 1 GHz†
Typical Amplitude	2.57 V _{pp} into 50 Ω, 5 V _{pp} into high Z	800 mV _{pp}
Rising/Falling Edge (20%, 80%)	270 ps, typical	180 ps, typical
Duty Cycle of output with Clock Generation as source	45% to 55%	45% to 55%
Available Sources	PXI_CLK10, 10 MHz OCXO, Clock Generation up to 50 MHz	Clock Generation, PXIe-DStarA Network‡
* Operation of low speed ClkOut above 50 MHz is possible however NI does not guarantee performance. Use ClkOutLS as the destination terminal to force NI-Sync to use the low speed driver above 50 MHz. † Operation above 1 GHz is possible but NI does not guarantee performance. ‡ Routing PXIe-DStarA to ClkOut requires routing through either Banks 0, 1, or 2. Refer to the PXIe_DSTARA Network section of Chapter 3, Hardware Overview, for additional information.		

PXI_CLK10 to ClkOut Delay	
Typical at 25 °C	20.2 ns
Maximum over temperature.....	47.75 ns

Figure A-7 shows the typical Low Speed ClkOut Amplitude performance, with a sample size of 19 modules.

Figure A-7. Typical Low Speed ClkOut Amplitude Performance

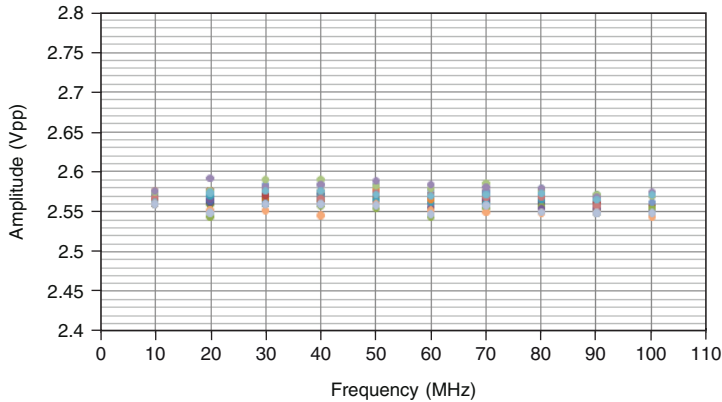
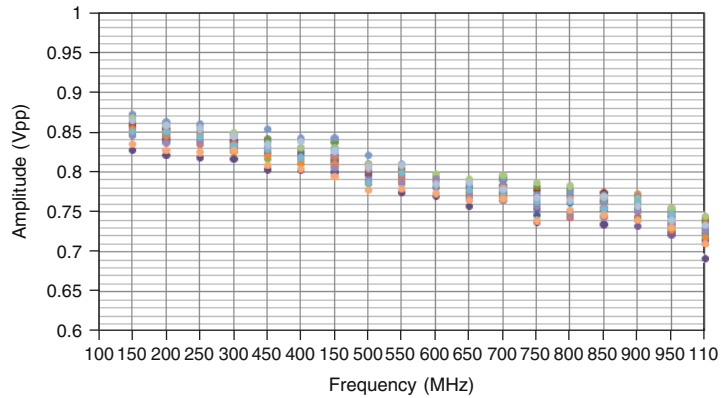


Figure A-8 shows the typical High Speed ClkOut Amplitude performance, with a sample size of 19 modules.

Figure A-8. Typical High Speed ClkOut Amplitude Performance



Clock Generation

Reference frequency source ¹	PXIe_Clk100
Base frequency resolution (150 MHz to 300 MHz)	2.84217 μ Hz ²
Minimum generated frequency ³	
With FPGA divider	0.2794 Hz
Without FPGA divider	4.6875 MHz
Maximum generated frequency	1 GHz ⁴

¹ Frequency Accuracy is inherited from PXIe_Clk100/PXI_Clk10. Use OCXO for PXIe_Clk100/PXI_Clk10 replacement for improved frequency accuracy and phase noise.

² This is the frequency resolution of the DDS used in the Clock Generation circuitry. For Clock Generation frequencies below 150 MHz, this resolution is divided down and for frequencies above 300 MHz, this resolution is multiplied up. Refer to the [Clock Generation](#) section in Chapter 3, [Hardware Overview](#), for more details.

³ When routed to ClkOut Low Speed or used as a trigger synchronization clock, Clock Generation can be further divided by the FPGA by factors of two up to 24. This extends the Clock Generation range down to 4.6875 MHz/ 2^{24} = .2794 Hz. When routed to ClkOut High Speed the minimum frequency is 4.6875 MHz. Use ClkOutHS as the destination terminal to force NI-Sync to use the low speed driver below 50 MHz. Note that AC coupling on ClkOut limits the minimum frequency which can be used.

⁴ Clock Generation can be operated beyond the upper limit; however, NI does not guarantee performance beyond 1 GHz. 2 GHz is the maximum output frequency by design.

Clock Generation Phase Noise Performance



Note All Phase Noise Measurements were made on a Representative Module of various Clock Generation frequencies routed to ClkOut. All Measurement made in an NI PXIe-1062 chassis with low fan speed and OCXO connected to PXI_Clk10_IN.

The phase noise performance of the clock generation circuitry varies depending on what elements are used to generate the requested frequency. To generate frequencies above 300 MHz, a PLL is used to multiply the DDS frequency up which results in increased phase noise versus when the DDS is used directly (all frequencies below 300 MHz).

Figure A-9. Phase Noise Performance

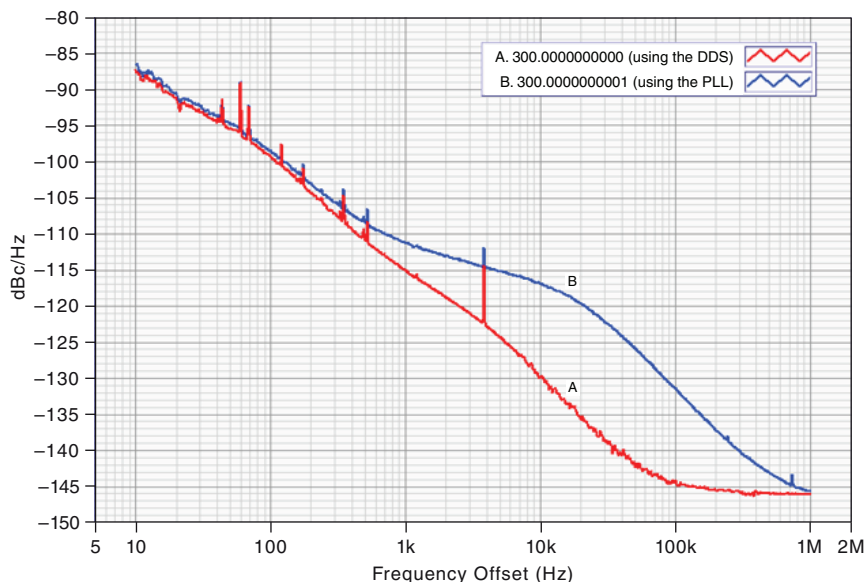
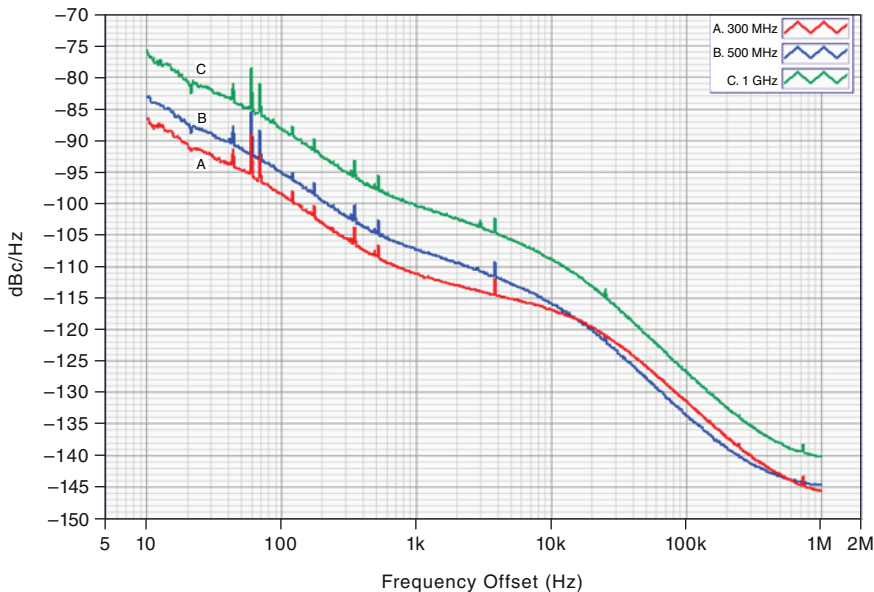


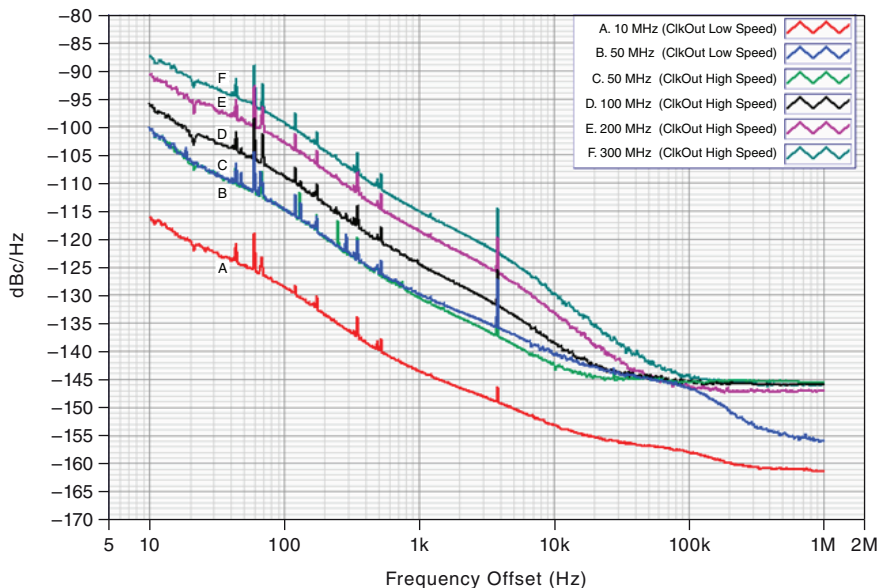
Figure A-10 shows the phase noise of various frequencies coming from the multiplying PLL.

Figure A-10. Phase Noise of Frequencies From the Multiplying PLL



At 50 MHz, NI-Sync software will automatically switch between the high speed and low speed ClkOut drivers¹. The phase noise performance of these two drivers differs, as shown in Figure A-11.

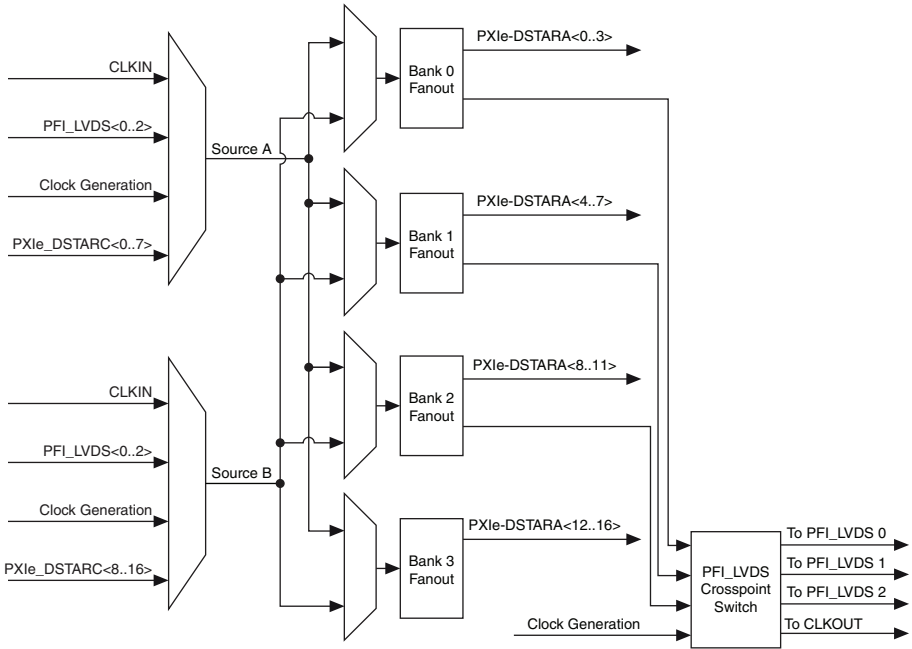
Figure A-11. Phase Noise of Frequencies from DDS



¹ Use ClkOutHS as the destination terminal to force NI-Sync to use the high speed driver below 50 MHz.

PXle-DStarA

Figure A-12. PXle-DStarA Topology



PXle-DStarA Maximum Frequency 1 GHz¹

PXle-DStarA LVPECL Signal Characteristics

	Minimum	Typical	Maximum
Voltage High Output	2.155 V	2.280 V	2.405 V
Voltage Low Output	1.355 V	1.530 V	1.700 V
Rise Time/Fall Time 20%, 80%	125 ps	180 ps	275 ps

ClkIn to PXle-DStarA Delay

- Typical at 25 °C 4.21 ns
- Maximum over temperature.....4.36 ns

PXle-DStarA to PXle-DStarA Skew

- Typical.....<100 ps
- Maximum over temperature.....250 ps

¹ Maximum Frequency may exceed 1 GHz however performance is not guaranteed.

Triggers

PFI Single Ended

Input Characteristics

Termination Setting	High Impedance	50 Ω
Input Impedance	10 k Ω , $\pm$ 20%	50 Ω , $\pm$ 5%
Input Coupling	DC	DC
Hysteresis	50 mV typical	58 mV typical (Revision C and D)** 53 mV typical (Revision E and later)**
Adjustable Threshold Range	15 mV to 3.795 V	16.8 mV to 4.25 V (Revision C and D)** 15.975 mV to 4.04 V (Revision E and later)**
Adjustable Threshold Resolution	15 mV	16.8 mV (Revision C and D)** 15.975 mV (Revision E and later)**
Adjustable Threshold Error*	$\pm$ 5 mV	$\pm$ 5 mV
Default Threshold Setting	1.005 V	1.008 V (Revision C and D)** 1.006 V (Revision E and later)**
Minimum Input Voltage Swing [†]	400 mV _{pp}	450 mV _{pp}
Frequency Range [‡]	DC to 150 MHz	DC to 150 MHz
Recommended Maximum Input Voltage Range	0.0 V to 5.0 V	0.0 V to 5.0 V
Maximum Input Voltage Range**	-0.5 V to 5.5 V	-0.5 V to 5.5 V
PFI Open Circuit Voltage ^{††}	0.45 V, typical	N/A
* PFI Input switching behavior is a function of both the threshold setting and hysteresis. [†] Input Voltage Swing below 400 mV may be possible but performance is not guaranteed. [‡] Operation beyond 150MHz frequency may be possible but performance is not guaranteed. ** Voltages beyond the maximum range may cause damage to the device. ^{††} PFI line will float to 0.45 V when configured in high impedance mode with no external signal connected as input. ^{‡‡} Ensure that the specifications of interest match the revision label on your board. The location of the label is shown in Figure A-1, NI PXIe-6674T Revision Label.		

Output Characteristics

Output Impedance	50 Ω , nominal
Output Coupling	DC
Output Voltage Range into 50 Ω load	0 V to 1.63 V, typical
Output Voltage Range into open load	0 V to 3.22 V, typical
Output Rising/Falling Edge into 50 Ω load	450 ps to 500 ps, 20%-80%, typical
Maximum Output Frequency*	DC to 150 MHz
* Operation beyond 150 MHz frequency may be possible but performance is not guaranteed.	

PFI LVDS

Input Characteristics

Minimum Differential Input Voltage	100 mV _{pp}
Recommended Maximum Differential Input Voltage*	1 V
Maximum Input Voltage Range [†]	0 V to 4 V
Differential Input Resistance	100 Ω , $\pm$ 10%
Maximum Input Frequency—Routed to DStarA [‡]	1 GHz
Maximum Input Frequency—Routed to FPGA**	200 MHz
* Operation with greater voltage swing will not damage the device but performance characteristics are not guaranteed. [†] Maximum Input Voltage Range is any combination of input voltage swing and common mode voltage. For example, a 200 mV differential swing with common mode voltage of 100 mV is acceptable as the lowest applied voltage to the input would be 0 V. A 200 mV differential swing with common mode less than 100 mV would cause the applied voltage to fall below 0 V and therefore would not be acceptable. [‡] Operation beyond 1 GHz is possible but performance is not guaranteed. ** Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS receiver.	

Output Characteristics

Differential Output Voltage into 100 ohm differential load (at DC)	600 mV _{pp} typical
Output Common Mode Voltage	1.125 V to 1.375 V
Maximum Output Frequency—Sourced from Cross Point Switch*	1 GHz
Maximum Output Frequency—Sourced from FPGA†	200 MHz
Differential Rise and Fall Time	180 ps, typical
* Operation beyond 1 GHz is possible but performance is not guaranteed.	
† Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS driver.	

Figure A-13 shows the representative LVDS output operating at 100 MHz. 1 unit interval in this figure equals 5 ns.

Figure A-13. Representative LVDS Output Operating at 100 MHz

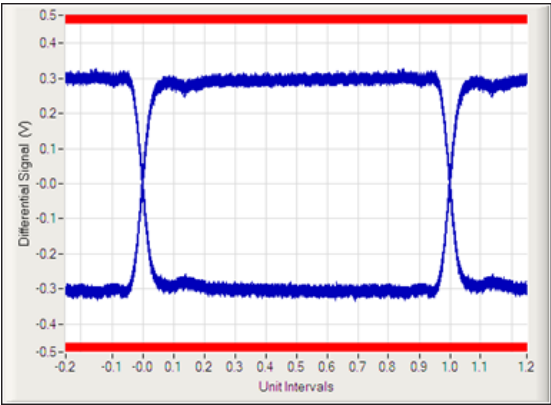
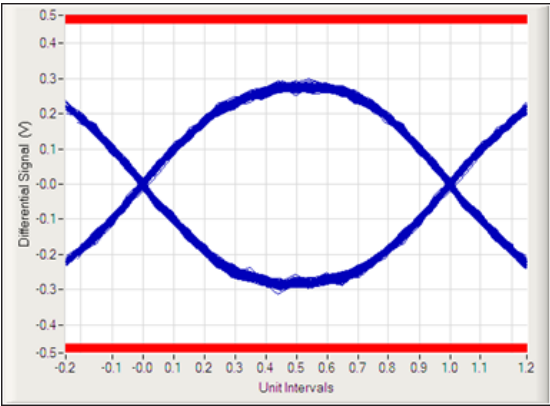


Figure A-14 shows the representative LVDS output operating at 1 GHz. 1 unit interval in the figure equals 500 ps.

Figure A-14. Representative LVDS output operating at 1 GHz



PXI-Triggers

I/O Voltage Level.....3.3 V CMOS, 5 V input tolerant

PXI-Star

I/O Voltage Level.....3.3 V CMOS, 5 V input tolerant

PXIe-DStarB

The PXIe-DStarB signals are LVDS signals that allow the NI PXIe-6674T to route high speed trigger signals to any other PXIe slot in a chassis. Each PXI Express slot in a chassis has its own PXIe-DStarB connection with the System Timing Slot.

By default, these are driven logic low until configured by software.

Maximum operating frequency.....200 MHz

PXIe-DStarC

The PXIe-DStarC signals are LVDS signals that come from other PXI Express slots in a chassis. Each PXI Express slot in a chassis has a PXIe-DStarC connection with the System Timing Slot. These allow other modules in a PXIe-Chassis to share a trigger or clock signal with the NI PXIe-6674T. The NI PXIe-6674T can connect a signal received through PXIe-DStarC to the PXIe-DStarA network (when sharing a clock signal) or treat the PXIe-DStarC as a trigger source.

Maximum operating frequency when used
with the PXIe-DStarA network.....1 GHz

Maximum operating frequency
when used for triggering.....200 MHz

Trigger Timing

Asynchronous Trigger Delays and Skew

Table A-1. Asynchronous Trigger Delays and Skew Values

Trigger Source	Trigger Destination	Typical Delay*	Typical Skew†
Single Ended PFI	Single Ended PFI	23.4 ns	<.5 ns
Single Ended PFI	LVDS PFI	22.4 ns	<.5 ns
Single Ended PFI	PXI-Trigger	38.7 ns	<1.5 ns
Single Ended PFI	PXI-Star	26.8 ns	<.75 ns
Single Ended PFI	PXIe-DStarB	23.2 ns	<.5 ns
LVDS PFI	Single Ended PFI	13.7 ns	<.5 ns
LVDS PFI	LVDS PFI	11.8 ns	<.5 ns
LVDS PFI	PXI-Trigger	28.9 ns	<1.5 ns
LVDS PFI	PXI-Star	17.5 ns	<.75 ns
LVDS PFI	PXIe-DStarB	13.8 ns	<.5 ns
PXI-Trigger	Single Ended PFI	17.8 ns	<.5 ns
PXI-Trigger	LVDS PFI	16.6 ns	<.5 ns
PXI-Trigger	PXI-Trigger	33.8 ns	<1.5 ns
PXI-Trigger	PXI-Star	21.0 ns	<.75 ns
PXI-Trigger	PXIe-DStarB	15.9 ns	<.5 ns
PXI-Star	Single Ended PFI	17.0 ns	<.5 ns
PXI-Star	LVDS PFI	15.6 ns	<.5 ns
PXI-Star	PXI-Trigger	26.2 ns	<1.5 ns
PXI-Star	PXI-Star	20.2 ns	<.75 ns
PXI-Star	PXIe-DStarB	16.0 ns	<.5 ns
PXIe-DStarC	Single Ended PFI	13.6 ns	<.5 ns
PXIe-DStarC	LVDS PFI	7.2 ns	<.5 ns
PXIe-DStarC	PXI-Trigger	28.1 ns	<1.5 ns

Table A-1. Asynchronous Trigger Delays and Skew Values (Continued)

Trigger Source	Trigger Destination	Typical Delay*	Typical Skew†
PXIe-DStarC	PXI-Star	16.8 ns	<.75 ns
PXIe-DStarC	PXIe-DStarB	13.0 ns	<.5 ns
* Typical Delay is measured from the input to the NI PXIe-6674T at the connector to the output at the connector. For example, Single Ended PFI to PXI-Star is the delay from the Single Ended PFI SMA connector to the PXI-Star at the backplane connector. † Typical Skew is defined as the difference in arrival time of a rising edge on a common source to two or more outputs with in a trigger destination, as seen as the connector. For example, if Single Ended PFI(0) is asynchronously routed to all PXI-Star lines, the typical skew would be less than .75 ns.			

Synchronized Trigger PXI_Clk10 to Out

Table A-2. Synchronized Trigger PXI_Clk10 to Out

Trigger Destination	Clock to Out Time*
Single Ended PFI	11.2 ns Typical, 19.9 ns Max
LVDS PFI	9.8 ns Typical, 14.8 ns Max
PXI-Trigger	28.2 ns Typical, 30.2 ns Max
PXI-Star	14.8 ns Typical, 24.5 ns Max
PXIe-DStarB	9.4 ns Typical, 14.0 ns Max
* Clock to Out Time is the amount of time it takes for a logic change on a synchronous trigger to appear (at the connector) with respect to the rising edge of PXI_Clk10 (at the backplane connector) that it is synchronized to. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.	

Synchronized Trigger Setup and Hold Timing with Respect to PXI_Clk10

Table A-3. Synchronized Trigger Setup and Hold Timing With Respect to PXI_Clk10

Trigger Source	Trigger Destination	Setup Time*	Hold Time†
Single Ended PFI	Single Ended PFI	11.2 ns Typical, 13.2 ns Max	-8.2 ns Typical, 1.1 ns Max
Single Ended PFI	LVDS PFI	11.2 ns Typical, 13.5 ns Max	-8.5 ns Typical, 0.8 ns Max
Single Ended PFI	PXI-Trigger	11.3 ns Typical, 14.2 ns Max	-7.5 ns Typical, 1.3 ns Max
Single Ended PFI	PXI-Star	11.2 ns Typical, 13.1 ns Max	-6.9 ns Typical, 2.0 ns Max
Single Ended PFI	PXIe-DStarB	13.2 ns Typical, 15.4 ns Max	-9.8 ns Typical, -0.4 ns Max
LVDS PFI	Single Ended PFI	0.6 ns Typical, 4.0 ns Max	0.4 ns Typical, 3.9 ns Max
LVDS PFI	LVDS PFI	-0.3 ns Typical, 4.3 ns Max	1.2 ns Typical, 3.5 ns Max
LVDS PFI	PXI-Trigger	-0.2 ns Typical, 3.6 ns Max	1.1 ns Typical, 5.0 ns Max
LVDS PFI	PXI-Star	-0.1 ns Typical, 3.7 ns Max	1.4 ns Typical, 5.0 ns Max
LVDS PFI	PXIe-DStarB	2.1 ns Typical, 5.7 ns Max	-0.5 ns Typical, 2.6 ns Max
PXI-Trigger	Single Ended PFI	11 ns Typical, 17.5 ns Max	-9.5 ns Typical, -4.8 ns Max
PXI-Trigger	LVDS PFI	10.9 ns Typical, 18.1 ns Max	-9.8 ns Typical, -5.4 ns Max
PXI-Trigger	PXI-Trigger	10.1 ns Typical, 17.0 ns Max	-7.8 ns Typical, -3.6 ns Max
PXI-Trigger	PXI-Star	9.7 ns Typical, 16.2 ns Max	--7.4 ns Typical, -3.1 ns Max

Table A-3. Synchronized Trigger Setup and Hold Timing With Respect to PXI_Clk10 (Continued)

Trigger Source	Trigger Destination	Setup Time*	Hold Time†
PXI-Trigger	PXIe-DStarB	10.7 ns Typical, 17.8 ns Max	-9.0 ns Typical, -5.1 ns Max
PXI-Star	Single Ended PFI	3.9 ns Typical, 10.9 ns Max	-2.5 ns Typical, -0.5 ns Max
PXI-Star	LVDS PFI	3.9 ns Typical, 11.1 ns Max	-3.1 ns Typical, -0.8 ns Max
PXI-Star	PXI-Trigger	2.7 ns Typical, 9.9 ns Max	-0.9 ns Typical, 0.9 ns Max
PXI-Star	PXI-Star	2.0 ns Typical, 9.6 ns Max	-0.1 ns Typical, 1.1 ns Max
PXI-Star	PXIe-DStarB	4.3 ns Typical, 11.7 ns Max	-2.4 ns Typical, -1.1 ns Max
PXIe-DStarC	Single Ended PFI	0.5 ns Typical, 3.9 ns Max	0.4 ns Typical, 3.7 ns Max
PXIe-DStarC	LVDS PFI	-0.3 ns Typical, 4.4 ns Max	0.5 ns Typical, 3.1 ns Max
PXIe-DStarC	PXI-Trigger	-1.1 ns Typical, 2.8 ns Max	1.9 ns Typical, 5.2 ns Max
PXIe-DStarC	PXI-Star	-0.5 ns Typical, 3.2 ns Max	3.1 ns Typical, 4.9 ns Max
PXIe-DStarC	PXIe-DStarB	1.3 ns Typical, 5.6 ns Max	0.2 ns Typical, 2.4 ns Max
* Setup Time is the amount of time before a rising edge of PXI_Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information. † Hold Time is the amount of time after a rising edge of PXI_Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.			

FPGA Functionality

Trigger Routing

Table A-4 shows the routes that can be made.

Table A-4. Sources and Destinations for NI PXIe-6674T Signal Routing Operations

		Destinations										
Sources			Front Panel			Backplane					On board	
			CLK OUT	PFI <0..5>	PFI LVDS <0..2>	PXI CLK 10 IN	PXI Star Trigger <0..16>	PXI TRIG <0..7>	PXIe SYNC CTRL	D STARA <0..16>	D STARB <0..16>	OCXO Ref PLL
	Front Panel	CLK IN	✓	✓†	✓†	✓	✓†	✓†		✓	✓†	✓
		PFI <0..5>		✓	✓		✓	✓	✓		✓	
		PFI LVDS <0..2>		✓	✓		✓	✓	✓	✓	✓	

Table A-4. Sources and Destinations for NI PXle-6674T Signal Routing Operations (Continued)

	Destination											
Sources	Backplane	PXI CLK 10	✓	✓†	✓†		✓†	✓†			✓†	
		PXI CLK 100	✓	✓†	✓†		✓†	✓†			✓†	
		PXI STAR <0..16>		✓	✓		✓	✓	✓		✓	
		PXI TRIG <0..7>		✓	✓		✓	✓	✓		✓	
		DSTARC <0..16>		✓	✓		✓	✓	✓	✓	✓	
	Onboard	OCXO	✓	✓†	✓†	✓	✓†	✓†			✓†	
		Clock Gen	✓	✓†	✓		✓†	✓†		✓	✓†	
		Global Software Trigger		✓	✓		✓	✓	✓		✓	
† Routing PXI_CLK10, PXIe_CLK100, OCXO or ClkGen is accomplished by setting the synchronization clock (NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.												
Route through the FPGA.												
Route to PFI LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DTARA network when used as a clock.												

Frequency Measurement

Maximum Measurable Frequency ¹	200 MHz
Reference Counter Source ²	PXIe_Clk100
Frequency Counter Sources.....	All Trigger inputs plus Clock In and the OCXO

Trigger Sync Clock

Two independent synchronization clock zones:

- Front Synchronization Clock for PFI Single Ended and PFI LVDS
- Rear Synchronization Clock for PXI-Star, PXI-Trigger, and PXIe-DStarB

Synchronization clock sources PXI_Clk10, PXIe_Clk100, Clock In, OCXO, and Clock Generation

Two division ratios can be specified in powers of 2 from 2 to 512. These ratios are used in all synchronization clock zones to divide down the selected full speed synchronization clock.

Physical

Chassis requirement.....	One 3U PXI Express slot (system timing slot)
Dimensions (not including connectors).....	16 cm × 10 cm (6.3 in. × 3.9 in.)
Front panel connectors.....	Eight SMA female, 50 Ω
Front panel indicators	Two tricolor LEDs (green, red, and amber)
Weight.....	349 g (12.3 oz)

Power Requirements

+3.3 V	2.54 A, max
+12 V	2.25 A, max
+5 V _{AUX}	0 A, max

Environmental

Maximum altitude.....	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2
Indoor use only.	

¹ Operation beyond 200 MHz is possible but performance is not guaranteed.
² Accuracy of frequency measurement is relative to the frequency accuracy of the reference counter source. The frequency measure vi in NI-Sync does not account for error from the reference source.

Operating Environment

Ambient temperature range	0 to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range.....	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range.....	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random vibration	
Operating	5 to 500 Hz, 0.3 g _{rms}
Nonoperating	5 to 500 Hz, 2.4 g _{rms} (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)



Caution Clean the NI PXIe-6674T module with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.



Note Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generates radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations and certifications, and additional information, refer to the [Online Product Certification](#) section.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity (DoC) for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）



中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

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- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer’s declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.

You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Symbol	Prefix	Value
f	femto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^3
M	mega	10^6
G	giga	10^9

Symbols

%	percent
$\pm$	plus or minus
+	positive, or plus
-	negative, or minus
/	per
$^{\circ}$	degree
Ω	ohm

A

accumulator	a part where numbers are totaled or stored
ADE	application development environment
asynchronous	a property of an event that occurs at an arbitrary time, without synchronization to a reference clock

B

backplane	an assembly, typically a printed circuit board (PCB), with 96-pin connectors and signal paths that bus the connector pins. PXI systems have two connectors, called the J1 and J2 connectors.
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An example of a PC bus is the PCI bus.

C

C	Celsius
CLKIN	CLKIN is a signal connected to the SMA input pin of the same name. CLKIN can serve as PXI_CLK10_IN or be used as a phase lock reference for the OCXO.
CLKOUT	CLKOUT is the signal on the SMA output pin of the same name.
clock	hardware component that controls timing for reading from or writing to groups
CompactPCI	a Eurocard configuration of the PCI bus for industrial applications

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device that converts a digital number into a corresponding analog voltage or current
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
DC	direct current
DDS	direct digital synthesis—a method of creating a clock with a programmable frequency

E

EEPROM electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed

ESD electrostatic discharge

F

frequency the rate of events or oscillations per second, measured with a frequency counter or spectrum analyzer. Frequency is the reciprocal of the period of a signal.

frequency tuning word a number that specifies the frequency generated by a DDS

front panel the physical front panel of an instrument or other hardware

H

Hz hertz—the number of scans read or updates written per second

I

in. inch or inches

J

jitter the variation in time of a clock or oscillator from its ideal timing

L

LabVIEW a graphical programming language

LED light-emitting diode—a semiconductor light source

LVDS Low Voltage Differential Signaling

M

master	the requesting or controlling device in a master/slave configuration
Measurement & Automation Explorer (MAX)	a controlled centralized configuration environment that allows you to configure all of your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices

N

NI-DAQ	National Instruments driver software for DAQ hardware
--------	---

O

OCXO	oven-controlled crystal oscillator
oscillator	a device that generates a fixed frequency signal. An oscillator most often generates signals by using oscillating crystals, but also may use tuned networks, lasers, or atomic clock sources. The most important specifications on oscillators are frequency accuracy, frequency stability, and phase noise.
output impedance	the measured resistance and capacitance between the output terminals of a circuit

P

PFI	Programmable Function Interface
PLL	phase-locked loop
precision	the measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
propagation delay	the amount of time required for a signal to pass through a circuit
PXI Express	PCI eXtensions for Instrumentation—An open implementation of CompactPCI Express that adds electrical features that meet the high-performance requirements of instrumentation applications by providing triggering, local buses, and system clock capabilities. PXI Express also offers two-way interoperability with CompactPCI Express products.

PXI star a special set of single-ended trigger lines in the PXI backplane for high-accuracy device synchronization with minimal latencies on each PXI slot

PXIe_DStarA, PXIe_DStarB, PXIe_DStarC high speed differential signal paths that connect the system timing slot to each PXI Express peripheral slot (up to 17 peripheral slots)

R

RTSI bus Real-Time System Integration bus—the NI timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions. In a PXI or PXI Express system these are referred to as the PXI-Triggers.

S

s seconds

skew the actual time difference between two events that would ideally occur simultaneously. Inter-channel skew is an example of the time differences introduced by different characteristics of multiple channels. Skew can occur between channels on one module, or between channels on separate modules (intermodule skew).

slave a computer or peripheral device controlled by another computer

slot the place in the computer or chassis in which a card or module can be installed

SMA sub miniature type A—a small coaxial signal connector that features a threaded connection

synchronous a property of an event that is synchronized to a reference clock

system timing slot the slot in a PXI Express system which can house a system timing module

T

t_{CtoQ}	clock to output time
t_{hold}	hold time
t_{pd}	propagation delay time
TRIG	trigger signal
trigger	a digital signal that starts or times a hardware event (for example, starting a data acquisition operation)
t_{setup}	setup time

V

V	volts
VI	virtual instrument

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